AF/2675
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Samson Huang	§	Group Art Unit:	2675
Serial No.:	09/493,319	§	Examiner:	Leland R. Jorgensen
Filed:	January 28, 2000	§		
For:	OPTICAL DISPLAY DEVICE HAVING A MEMORY TO ENHANCE REFRESH OPERATIONS	§	Atty. Dkt. No.:	ITL.0312US (P7995)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Dear Sir:

Applicant submits the following reply to the Examiner's Answer.

I. CLAIMS APPEALED

The application was originally filed with claims 1-18. Claims 19-54 were added during prosecution; and claims 1-44 were cancelled during prosecution. Claims 45-54 have been finally rejected and are the subject of this appeal.

Date of Deposit: December 23, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop **Appeal Brief-Patents**, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Janice Munoz

II. REPLY TO EXAMINER'S ARGUMENTS

The Examiner still fails to establish a *prima facie* case of obviousness for any of the § 103 rejections for at least the following reasons. First, as previously pointed out, the Examiner fails to establish a *prima facie* case of obviousness for independent claims 45 and 50 for at least the reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation for the modification of Nakajima's integrated display device in view of Nishida. In response to Applicant's assertion that the Examiner provided no support as to why modifying Nakajima's integrated display device in the manner set forth by the Examiner would reduce the cost and complexity of Nakajima's device, the Examiner states, "Applicant's assertion that reducing the memory elements may increase the cost and complexity of the circuit is unfounded." Examiner's Answer, 4. However, it is not the Applicant's burden to disprove an untenable position taken by the Examiner. Mainly, the Examiner has failed to show where the prior art contains the alleged suggestion that modifying Nakajima's integrated display device in the manner contended by the Examiner would reduce the cost and complexity of this device. Instead, the Examiner is applying hindsight reasoning to justify the hypothetical combination of Nishida and Nakajima. Such hindsight reasoning, however, does not constitute a *prima facie* case of obviousness.

In response to Applicant's argument that the Examiner has failed to show where the combination of references teaches or suggests a memory buffer that is located closer to an associated group of pixel cells than another group of pixel cells, the Examiner now relies on inherency. For a limitation to be inherent in a reference, the limitation must *necessarily flow* from the reference. *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988).

Contrary to the requirements of inherency, the Examiner fails to show why locating a memory buffer closer to an associated group of pixel cells than another group of pixel cells necessarily flows from the teachings of either Nakajima or Nishida. The Examiner states, "it is inherent that a memory embedded in a pixel would be closer to the pixel than to other pixels." Examiner's Answer, 4. The Examiner then makes a conclusion that locating a memory buffer closer to one group of pixel cells than another group of pixel cells is somehow inherent. The Examiner does not, however, set forth why such a location necessarily flows from the cited art. Thus, it is entirely possible that such a relationship does not exist in the combination of Nakajima and Nishida, as the device derived from the hypothetical combination would certainly function as intended without the locations that are specifically set forth in independent claims 45 and 50.

Thus, for at least the reasons above, Applicant submits that the § 103(a) rejections of claims 45-54 are in error and should be reversed. The Commissioner is authorized to charge any fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0312US).

Respectfully submitted,

Date: December 23, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

45. A method comprising:

providing a light modulator comprising an array of pixel cells and memory buffers, each memory buffer being associated with a different group of two or more of the pixel cells and each memory buffer being located closer to the associated group of pixel cells than another one of the group of pixel cells; and

during a refresh operation, converting the digital indications stored in the memory buffers into analog voltages to update charge intensities on the pixel cells.

46. The method of claim 45, wherein the memory buffers are localized to the different groups.

47. The method of claim 45, wherein the memory buffers comprise ~~a~~ static random access memories.

48. The method of claim 45, further comprising:

during the refresh operation, reading the digital indications from the memory buffers.

49. The method of claim 45, further comprising:

during the refresh operation, latching the digital indications.

50. A light modulator comprising:

an array of pixel cells;

memory buffers being spatially distributed among the pixel cells, each memory buffer being associated with a different group of two or more of the pixel cells and storing ~~a~~ digital indications of associated predetermined voltages; and

digital-to-analog converters to convert the digital indications into analog voltages to update charges on the pixel cells during a refresh operation.

51. The light modulator of claim 50, wherein the refresh operation occurs at a different rate than a frame update operation to the pixel cells.

52. The light modulator of claim 50, wherein at least one of the memory buffers comprise static random access memory.

53. The method of claim 45, wherein each of the pixel cells is controlled independently with respect to the other pixel cells.

54. The light modulator of claim 50, wherein each of the pixel cells is controlled independently with respect to the other pixel cells.